CLAIMS

What is claimed is:

1. A system, comprising:

a first circuit having first sampling rate, wherein first circuit digitizes an inputted analog signal into an outputted first digital signal;

a second circuit having second sampling rate less than first sampling rate and having input connected to first circuit input, wherein second circuit digitizes the inputted analog signal into an outputted second digital signal and wherein when frequency of a first component of the inputted analog signal is less than half of first sampling rate and greater than half of second sampling rate, second circuit outputs an aliased component folded into an aliased frequency less than half of the second sampling rate and first circuit outputs a non-aliased component;

an anti-aliasing circuit having a first output and having input connected to first circuit output, wherein anti-aliasing circuit converts the non-aliased component to approximate amplitude of aliased component and folds into the aliased frequency at first output; and

a subtracter having inputs separately connected to second circuit output and to first output, wherein subtracter outputs first output subtracted from second circuit output.

2. The system as recited in claim 1, wherein the first circuit comprises a first analog circuit and a first analog-to-digital converter, wherein the input of the first analog circuit is connected to the input of the first circuit, wherein

the output of the first analog circuit is connected to the input of the first analog-to-digital converter, wherein the output of the first analog-to-digital converter is connected to the output of the first circuit, wherein the first analog circuit transforms the analog signal via an analog operation on the analog signal and outputs that transformed analog signal at the output of the first analog circuit, and wherein the first analog-to-digital converter digitizes the transformed analog signal input into the first digital signal and outputs the first digital signal at the output of the first analog-to-digital converter.

3. The system as recited in claim 1, wherein the first circuit comprises a first analog-to-digital converter and wherein the first analog-to-digital converter digitizes the inputted analog signal into the first digital signal.

4. The system as recited in claim 1, wherein the second circuit comprises a second analog circuit and a second analog-to-digital converter, wherein the input of the second analog circuit is connected to the input of the second circuit, wherein the output of the second analog circuit is connected to the input of the second analog-to-digital converter, wherein the output of the second analog-to-digital converter is connected to the output of the second circuit, wherein the second analog circuit transforms the analog signal via an analog operation on the analog signal and outputs that transformed analog signal at the output of the second analog circuit, and wherein the second analog-to-digital converter digitizes the transformed analog signal input into the second digital signal and outputs the second digital signal at the output of the second analog-to-digital converter.

5. The system as recited in claim 1, wherein the second circuit comprises a second analog-to-digital converter and wherein the second analog-to-

digital converter digitizes the inputted analog signal into the second digital signal.

6. The system as recited in claim 1, further comprising:

a merge circuit, wherein the anti-aliasing circuit further comprises a second output, wherein the anti-aliasing circuit outputs a high-pass filtered first digital signal at second output, wherein the merge circuit comprises inputs separately connected to the second output of the anti-aliasing circuit and subtracter output, and wherein merge circuit merges signal received at the merge circuit input connected to the output of the subtracter and the high-pass filtered first digital signal received at the merge circuit input connected to the second output of the anti-aliasing circuit.

7. The system as recited in claim 6, wherein the anti-aliasing circuit comprises:

a first high-pass filter having input connected to the input of the anti-aliasing circuit and output connected to the second output, wherein pass-band of the first high-pass filter passes frequencies greater than a preselected frequency less than half the second sampling rate;

a second high-pass filter having input connected to the input of the anti-aliasing circuit, wherein pass-band of the second high-pass filter passes frequencies greater than another preselected frequency less than half the second sampling rate; and

a compressor having input connected to the output of the second high-pass filter and output connected to the first output, wherein the

compressor folds the filtered non-aliased component from the second high-pass filter having frequency less than half the second sampling rate into the aliased frequency.

8. The system as recited in claim 6, wherein the anti-aliasing circuit comprises:

a first high-pass filter having input connected to the input of the anti-aliasing circuit and output connected to the second output, wherein pass-band of the first high-pass filter passes frequencies greater than a preselected frequency less than half the second sampling rate;

a compensation filter having input connected to the input of the anti-aliasing circuit, wherein the compensation filter has a transfer function approximating the ratio of the transfer function of the second circuit to the transfer function of the first circuit;

a second high-pass filter having input connected to the output of the compensation filter, wherein pass-band of the second high-pass filter passes frequencies greater than another preselected frequency less than half the second sampling rate; and

a compressor having input connected to the output of the second high-pass filter and output connected to the first output, wherein the compressor folds the filtered non-aliased component from the second high-pass filter having frequency less than half the second sampling rate into the aliased frequency.

9. The system as recited in claim 6, wherein the anti-aliasing circuit comprises:

a first high-pass filter having input connected to the input of the anti-aliasing circuit and output connected to the second output, wherein pass-band of the first high-pass filter passes frequencies greater than a preselected frequency less than half the second sampling rate; and

a compressor having input connected to the second output and output connected to the first output, wherein the compressor folds the filtered non-aliased component from the first high-pass filter having frequency less than half the second sampling rate into the aliased frequency.

10. The system as recited in claim 6, wherein the anti-aliasing circuit comprises:

a first high-pass filter having input connected to the input of the anti-aliasing circuit and output connected to the second output, wherein pass-band of the first high-pass filter passes frequencies greater than a preselected frequency less than half the second sampling rate;

a compensation filter having input connected to the second output, wherein the compensation filter has a transfer function approximating the ratio of the transfer function of the second circuit to the transfer function of the first circuit; and

a compressor having input connected to output of the compensation filter and output connected to the first output, wherein the compressor folds the filtered non-aliased component from the first high-pass filter having frequency less than half the second sampling rate into the aliased frequency.

11. The system as recited in claim 6, wherein the merge circuit comprises:

an interpolator having input connected to the input of the merge circuit that is connected to the subtracter, wherein the interpolator is configured such that the data rate at its output matches the data rate of the anti-aliasing circuit at the second output; and

a summation circuit having one input connected to the input of the merge circuit that is connected to the second output of the anti-aliasing circuit and the other input connected to the output of the interpolator.

12. The system as recited in claim 11, wherein the interpolator comprises:

an interpolation filter, wherein output of the interpolation filter is connected to output of the interpolator; and

an expander, wherein output of the expander is connected to the input of the interpolation filter, wherein input of the expander is connected to the input of the interpolator, wherein the expander matches the data rate at its input to that of the output of the anti-aliasing circuit, and wherein the interpolation filter is a low-pass filter capable of rejecting frequency-scaled images created by the expander.

13. The system as recited in claim 6, wherein the merge circuit comprises:

a flattening filter having input connected to the input of the merge circuit that is connected to the subtracter, wherein the flattening filter has a transfer function approximating the inverse of the transfer function of the second circuit;

an interpolator having input connected to the output of the flattening filter, wherein the interpolator is configured such that the data rate at its

output matches the data rate of the anti-aliasing circuit at the second output; and

a summation circuit having one input connected to the input of the merge circuit that is connected to the second output and the other input connected to the output of the interpolator.

14. The system as recited in claim 6, wherein the merge circuit comprises:

a decimator, wherein input of the decimator is connected to the input of the merge circuit that is connected to the second output and wherein the decimator is configured such that the data rate at its output matches the data rate of the output of the subtracter; and

a summation circuit having one input connected to output of the decimator and another input connected to output of the subtracter.

15. The system as recited in claim 6, wherein the merge circuit comprises:

a decimator, wherein input of the decimator is connected to the input of the merge circuit that is connected to the second output;

an interpolator having input connected to the input of the merge circuit that is connected to the subtracter, wherein the interpolator and the decimator are configured such that the data rates at output of the interpolator matches the data rate of the output of the decimator; and

a summation circuit having one input connected to output of the decimator and the other input connected to the output of the interpolator.

16. The system as recited in claim 6, wherein the merge circuit comprises:

a decimator, wherein input of the decimator is connected to the input of the merge circuit that is connected to the second output;

a flattening filter having input connected to the input of the merge circuit that is connected to the subtracter, wherein the flattening filter has a transfer function approximating the inverse of the transfer function of the second circuit;

an interpolator having input connected to the output of the flattening filter, wherein the interpolator and the decimator are configured such that the data rates at output of the interpolator matches the data rate of the output of the decimator; and

a summation circuit having one input connected to output of the decimator and the other input connected to the output of the interpolator.

17. The system as recited in claim 16, wherein the interpolator comprises:

an interpolation filter, wherein output of the interpolation filter is connected to output of the interpolator; and

an expander, wherein output of the expander is connected to the input of the interpolation filter, wherein input of the expander is connected to the input of the interpolator, wherein the expander matches the data rate at its input to that of the output of the anti-aliasing circuit, and wherein the interpolation filter is a low-pass filter capable of rejecting frequency-scaled images created by the expander.

18. A method for analog-to-digital conversion, comprising:

digitizing an input analog signal using a first sampling rate;

digitizing an input analog signal using a second sampling rate, wherein the first sampling rate is faster than the second sampling rate;

removing low frequency components from the result of digitizing using the first data rate;

replicating the result of the removal step at an appropriate signal strength;

folding the result of the replication step into appropriate frequencies;

subtracting the result of the folding step from the result of the step digitizing the input analog signal using the second sampling rate; and

merging the result of the subtraction step and the result of the removal step.

19. The method as recited in claim 18, further comprising correcting the signal strength resultant from the subtraction step prior to the merging step.